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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,707	09/24/2003	Chung-Che Tsai	MM4639	6133

7590 04/04/2005

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,707	TSAI, CHUNG-CHE	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *10-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed 17 March 2005.

Election/Restrictions

Claims 10-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected method of making a semiconductor device, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 17 March 2005.

Applicant's election without traverse of claims 1-9 in the reply filed on 17 March 2005 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 5-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Applicant's Prior Art (Figs. 4a-4f).

Applicant's Prior Art (Figs. 4a-4f) disclose a window ball grid array that contains a substrate (10) having an upper surface (100) and an opposite lower surface (101) and having an opening (102) formed through the same; at least one chip (11) mounted on the upper surface and over the opening of the substrate via an adhesive (12), and electrically connected to the lower surface of the substrate via a plurality of bonding wires (13) going through the opening, with gaps (G), not applied with the adhesive, being formed between the chip and the substrate; an encapsulation body (14/15) made of a resin material and formed on the upper and lower surfaces of the substrate for encapsulating the chip and the bonding wires, wherein the gaps between the chip and the substrate allow the resin material to pass there through to fill the opening of the substrate and the gaps; and a plurality of solder balls (16) bonded to area free of the encapsulation body on the lower surface of the substrate and exposed outside, where the encapsulation body partly formed on lower surface of the substrate has a thickness smaller than the height of the solder balls, and the chip has an active surface and an opposite inactive surface where the active surface faces the opening and is connected by bonding wires allowing the active surface to be entirely encapsulated by the adhesive and encapsulation body, the surface area of the chip is larger than the opening of the substrate and entirely covers the opening, where the opening is of a rectangular shape having two opposite longer sides and two opposite shorter sides, wherein the gaps between the chip and substrate are located along the two shorter sides of the opening (Fig. 4a) and have a height equal to the thickness of the adhesive.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al. (U.S. Patent 6,528,722).

Huang discloses a ball grid array (Figs. 1 and 8) that contains a substrate (52) having an upper surface (524) and an opposite lower surface (525) and having an opening formed through the same; at least one chip (53) mounted on the upper surface and over the opening of the substrate via an adhesive (57), and electrically connected to the lower surface of the substrate via a plurality of bonding wires (54) going through the opening, with gaps (area between chip and substrate on the side of the adhesive), not applied with the adhesive, being formed between the chip and the substrate; an encapsulation body (55) made of a resin material and formed on the upper and lower surfaces of the substrate for encapsulating the chip and the bonding wires, wherein the gaps between the chip and the substrate allow the resin material to pass there through to fill the opening of the substrate and the gaps; where the inactive surface of the chip is exposed to the outside of the encapsulation body (Fig. 8) and a plurality of solder balls (56) bonded to area free of the encapsulation body on the lower surface of the substrate and exposed outside, where the encapsulation body partly formed on lower surface of the substrate has a thickness smaller than the height of the solder balls, and the chip has an active surface and an opposite inactive surface where the active surface faces the opening and is connected by bonding wires allowing the active surface to be entirely encapsulated by the adhesive and encapsulation body, the surface area of the chip is larger than the opening of the substrate and entirely covers the opening, where the

opening is of a rectangular shape having two opposite longer sides and two opposite shorter sides, wherein the gaps have a height equal to the thickness of the adhesive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (Figs. 4a-4f) in view of Huang.

Applicant's Prior Art discloses all the limitations except for the inactive surface of the chip being exposed from the encapsulation body. Whereas Huang discloses a ball grid array (Fig. 8) that contains a substrate (52), a chip (53') with an active surface (531) and an inactive surface (opposite side) and an encapsulation body (55') wherein the inactive surface of the chip is exposed to the outside of the encapsulation body. The inactive surface of the chip is exposed from the encapsulation body to dissipate heat to the atmosphere via the inactive surface of the chip and therefore the heat dissipating efficiency is improved. (Column 5, lines 53-67 and Column 6, lines 1-3) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Applicant's Prior Art (Figs. 4a-4f) by incorporating the inactive surface of the chip exposed from the encapsulation body to dissipate heat to

the atmosphere via the inactive surface of the chip and therefore the heat dissipating efficiency is improved as taught by Huang.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

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